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UTILITY APPLICATION FOR UNITED STATES PATENT

FOR

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Inventor(s):
Dae-Young Kim

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025
Telephone: (310) 207-3800

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Field of Invention

The present invention relates to a method of fabricating a semiconductor device; and, more particularly, to a method of fabricating a semiconductor device for effectively protecting a punchthrough phenomenon.

Description of Related Art

According to high integration of a semiconductor device, an occupied area of a transistor is reduced because a cell area is reduced. So, a channel length between source and drain of the transistor becomes shorter. However, a high electric field exists between the source and the drain of the transistor because of reduction of the channel length. This is known as a punchthrough phenomenon, that is, when two depletion areas are joined by a high electric field.

Summary of Invention

For solving the punchthrough problem of the prior art, it is, therefore, an object of the present invention to provide a method of fabricating a semiconductor device for effectively eliminating the punchthrough phenomenon between source and drain of a transistor in a highly integrated

semiconductor device.

In accordance with an aspect of the present invention, there is provided a method of fabricating a semiconductor device which includes the step of forming a source and a drain doped with a first conductivity type in an active area, which is made on both sides of a word line by an isolation layer of a second conductivity type doped substrate. Each word line is separated by a predetermined interval. Then, a first contact and a second contact are formed using the isolation layer which is separated at a wider interval on the source than on the drain to expose the source and the drain; and selectively implanting the second conductivity type dopant ion in the source by using the isolation layer and the word line as an ion implanting mask during a tilt ion implantation process.

Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a top plan view of a semiconductor device in accordance with a preferred embodiment of the present invention;

Fig. 2 is a cross-sectional view of the semiconductor device taken by a line II-II' shown in Fig. 1;

Fig. 3 is a cross-sectional view of the semiconductor

device taken by a line III-III' shown in Fig. 1;

Fig. 4 is a cross-sectional view of the semiconductor device taken by a line IV-IV' shown in Fig. 1;

Fig. 5 describes simulation result about junction of source and drain of the transistor in accordance with the prior art; and

Fig. 6 is an explanatory diagram illustrating a simulation result about junction of source and drain of the transistor contained in a semiconductor device in accordance with the present invention.

Detailed Description of the Invention

Hereinafter, a method of fabricating a semiconductor device according to the present invention will be described in detail referring to the accompanying drawings.

Figs. 1 to 4 are a plan and cross-sectional views for describing a method of fabricating a semiconductor device in accordance with a preferred embodiment of the present invention. Fig. 2 is a cross-sectional view of the semiconductor device taken by a line II-II' shown in Fig. 1. Fig. 3 is a cross-sectional view of the semiconductor device across a line III-III' shown in Fig. 1. Fig. 4 is a cross-sectional view of the semiconductor device taken by a line IV-IV' shown in Fig. 1.

Referring to Figs. 1 to 4, the word line 12 is composed of a hard-mask, a gate, and a gate-insulation layer formed in

predetermined intervals on an active area A of a substrate 10 by a device isolation layer. Herein, the hard-mask is made of a nitride layer and the gate is made of a metal/poly-silicon or metal-silicide/poly-silicon lamination layer. Then, a junction between source and drain in the active area A is formed by implanting an N type dopant ion on both sides of the word line 12 of the substrate 10. The source 13 is connected to a bit line and the drain 14 is connected to a storage node of a capacitor.

The isolation layer 16 is formed for separating the semiconductor device at a predetermined interval and perpendicularly crossing the semiconductor device to the word line 12. First and second contact holes 17A and 17B for a landing plug contact LPC for exposing the source 13 and the drain 14 of the transistor are formed. As the isolation layer 16 is more widely arranged in the source 13 of the transistor than in the drain 14 of the transistor, a size of the first contact hole 17A is relatively large because there is opened not only a whole area of the source 13 but also a partial area of the isolation layer 11 adjacent to the source 13.

Using a mask for ion implantation, a tilt ion implantation process is performed in the isolation layer 16 and the word line 12 to implant a P-type dopant ion, e.g., Boron, in a preferred embodiment- in the source 13 of the transistor. The tilt ion implantation process is carried out using a tilt angle of about 20° to about 25° and, preferably, a twist of about 7° to 18°. Also, the tilt ion implantation

process is carried out in a direction of the word line 12. Because the interval between the isolation layers 16 is wider in the source 13 of the transistor than in the drain 14 of the transistor, the dopant density of the source 13 is weaker than that of the drain 14 and a doping depth 13A of the source 13 is shallower than that of the drain 14. After the above processes, there are performed processes for forming a landing plug contact LPC, a bit line contact, and a storage node contact.

In the above embodiment, the tilt ion implantation process is carried out by using the isolation layer which is arranged at different intervals on the source and the drain of the transistor so that the punchthough phenomenon between the source 13 and the drain 14 of the transistor is effectively eliminated by reducing the doping depth of the source 13.

Fig. 5 describes simulation results for a junction of source and drain of a transistor contained in a conventional semiconductor device and Fig. 6 describes simulation results for a junction of source and drain of the transistor contained in a semiconductor device in accordance with the present invention.

In the present invention, the P-type dopant is implanted in the source of the transistor by the tilt ion implantation process. As shown in Figs. 5 and 6, the source S2 of the transistor in accordance with the present invention has a shallower doping depth than does source S1 in accordance with the prior art. Because the source S2 of the transistor has a

shallower doping depth, it is difficult to join the source S2 to the drain of the transistor by reducing a junction area of the source S2.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.